jc713 U.S. PTO
01/28/00

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	684.2961
First Named Inventor or Application Identifier	AKIHIRO OUCHI
Express Mail Label No.	

jc511 U.S. PTO
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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. [X] Specification — *Total Pages* 21

3. [X] Drawing(s) *(35 USC 113)* — *Total Sheets* 6

4. [X] Oath or Declaration — *Total Pages* 1

   a. [ ] Newly executed (original or copy)
   b. [X] Unexecuted for information purposes
   c. [ ] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed Statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation By Reference *(useable if Box 4c is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4c, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program *(Appendix)*

7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))

9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney

10. [ ] English Translation Document *(if applicable)*

11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations

12. [ ] Preliminary Amendment

13. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application Status still proper and desired

15. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)

16. [ ] Other: _____

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No. _____

18. CORRESPONDENCE ADDRESS

[X] Customer Number or Bar Code Label — 05514 (Insert Customer No. or Attach bar code label here) — or [ ] Correspondence address below

NAME					
Address					
City		State		Zip Code	
Country		Telephone		Fax	

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	4-20 =	0	X $ 18.00 =	$ 0.00
	INDEPENDENT CLAIMS (37 cfr 1.16(b))	1-3 =	0	X $ 78.00 =	$ 0.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			$ 260.00 =	$ 0.00
				BASIC FEE (37 CFR 1.16(a))	$ 690.00
			Total of above Calculations =		$ 690.00
	Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				
				TOTAL =	$ 690.00

19. Small entity status
    - a. ☐ A Small entity statement is enclosed
    - b. ☐ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
    - c. ☐ Is no longer claimed.

20. ☒ A check in the amount of $ 690.00 to cover the filing fee is enclosed.

21. ☐ A check in the amount of $ _____ to cover the recordal fee is enclosed.

22. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 06-1205:
    - a. ☒ Fees required under 37 CFR 1.16.
    - b. ☐ Fees required under 37 CFR 1.17.
    - c. ☐ Fees required under 37 CFR 1.18.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED	
NAME	Scott D. Malpede - Reg. No. 32,533
SIGNATURE	Scott D. Malpede
DATE	January 28, 2000

SDM\lmj

PICTURE DISPLAY APPARATUS

FIELD OF THE INVENTION AND RELATED ART

The present invention relates to a dot matrix-type picture display apparatus with a new type of display picture position adjustment means, particularly suitable for a multiscan-type liquid crystal display or liquid crystal projector to which picture signals of indefinite signal format are inputted.

In recent years, as picture display apparatus for computer apparatus, etc., those of the so-called multiscan-type capable of displaying picture signals having various frequencies (or resolutions) become popular. In this regard, picture signals inputted from the exterior are not always of a prescribed single format, but even picture signals having an identical resolution can have different horizontal or vertical initial or starting points of display on an entire display picture area or a display panel. This means that the deviation in starting point of display can lead to a lack of display picture in the case of a dot matrix-type picture display apparatus wherein a picture display region corresponds to a number of display pixels. Accordingly, the picture display apparatus is required to have a means for displaying a picture at an exact position corresponding to inputted

picture signal.

Figure 5 is a block diagram showing an organization of a conventional picture display apparatus. Referring to Figure 5, the picture display apparatus includes an A/D converter 1, a picture display unit drive circuit 2, a picture display unit 3, a display control circuit 4, and a preset data memory 5. Based on the organization, analog video signals Ra, Ga and Ba are converted by the A/D converter 1 into digital signals Rd, Gd and Bd, which are then stored at a picture memory contained within the picture display unit drive circuit 2. The time of writing in the picture memory is controlled by the display control circuit 4. At the picture display unit drive circuit 2, picture data processing for producing signals R, G and B suitable for the picture display unit 3 is effected, and drive timing pulses (horizontal synchronizing pulses H, vertical synchronizing pulses V and pixel clock signals CK) are generated. In this organization, the display position adjustment is performed by storing preset picture position data based on expected input signal formats in the preset data memory 5, and judging the inputted signal format by the display control circuit 4 to set the picture display position to the preset value. Accordingly, an accurate position adjustment is impossible for inputted signals other than expected

input signals, so that there is provided an adjustment means for allowing an operator to effect a manual position adjustment.

Figure 6 is a block diagram of another example of conventional picture display apparatus, which includes an A/D converter 1, a picture display unit drive circuit 2, a picture display unit 3, a display control circuit 4, and a picture position detection circuit 6'. Based on this organization, the picture position detection circuit 6' is supplied with converted digital video signals Rd, Gd and Bd, a horizontal synchronizing signal H_{SYNC}, a vertical synchronizing signal V_{SYNC} and a dot clock signal DCK. By detecting positions of digital video signals Rd, Gd and Bd corresponding to the horizontal synchronizing signal H_{SYNC} and the vertical synchronizing signal V_{SYNC} by the position detection circuit 6' and based on the results thereof, the display control circuit 4 controls the timing for writing the digital video signals Rd, Gd and Bd in a picture memory contained in the picture display unit control circuit 2, thereby automatically adjusting the picture display position on the display unit (Japanese Laid-Open Patent Application (JP-A) 7-44125 and JP-A 10-63234).

The picture display apparatus of Figure 5 unnecessitates a manual adjustment for signal formats for which preset values have been set, but for signals

of other formats, the operator is required to effect a troublesome manual adjustment of horizontal and vertical positions while observing a picture displayed on the display unit and the adjustment is also difficult. On the other hand, the picture display apparatus of Figure 6 allows an automatic positional alignment but in view of higher resolution and higher input signal frequency adopted in recent years, the operation speed of the picture position detection circuit 6' is increased correspondingly to result in an increased current flow and a higher-speed expensive circuit device for realizing the picture position detection circuit 6', thus incurring an increased production and running cost. Particularly, in the case of effecting the picture position adjustment dot by dot, a substantial time is required for display position adjustment to cause a delay in commencement of display.

SUMMARY OF THE INVENTION

In view of the above-mentioned problem of the prior art, a principal object of the present invention is to provide a picture display apparatus equipped with means for detection and automatic adjustment of display position at a reduced current consumption and at a low cost in a dot matrix-type picture display apparatus.

According to the present invention, there is provided a picture display apparatus for displaying a picture in response to inputted picture signals of arbitrary format, comprising:

a picture display apparatus having an arranged matrix of dots for picture display,

picture display unit drive means for converting inputted picture signals into display picture signals adapted for display on the picture display unit and generating drive timing signals for driving the picture display unit,

display position detection means for detecting a picture display position on the picture display unit based on the display picture signals and the drive timing signals, and

display position control means for controlling admission of the inputted picture signals to the picture display unit drive means based on the detected display position data from the display position detection means.

These and other objects, features and advantages of the present invention will become more apparent upon a consideration of the following description of the preferred embodiments of the present invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an embodiment of the picture display apparatus according to the invention.

Figure 2 is a time chart for illustrating an example of display position relative to a horizontal synchronizing signal.

Figure 3 is a time chart for illustrating an example of display position relative to a vertical synchronizing signal.

Figure 4 is a flow chart illustrating a system flow of display position adjustment for the apparatus of Figure 1.

Figures 5 and 6 are respectively a block diagram of a conventional picture display apparatus including a picture display adjustment system.

Figure 7 is a time chart illustrating an example of outputted picture data.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1 showing an embodiment of the picture display apparatus according to the present invention, the picture display apparatus includes a picture display unit 3, an A/D conversion circuit 1 for converting inputted analog picture signals Ra, Ga and Ba into digital signals Rd, Gd and Bd, a picture display unit drive circuit 2 for

converting the digitally converted video signals Rd, Gd and Bd into display picture signals R, G and B suitable for displaying on the picture display unit 3 and generating drive timing signals for driving the picture display unit 3, a display picture detection circuit 6 for receiving the digital picture signals R, G and B, a horizontal synchronizing signal H, a vertical synchronizing signal V and pixel clock signals CK for the picture display unit 3 prepared by the picture display unit drive circuit 2 to detect horizontally initial and final points and vertically initial and final points for a display picture on the picture display unit 3, a display control circuit 4, and a preset data memory 5, wherein the timing for writing the digital signals Rd, Gd and Bd into a picture memory 2m contained in the picture display unit drive circuit 2 is controlled based on the display position detection circuit 6, thereby automatically adjusting a display picture position.

Further, by disposing the display position detection circuit 6 at a later stage than the picture display unit drive circuit 2, the operation speed of the display position detection circuit 6 is restricted within the drive speed of the picture display unit 3, whereby the detection circuit 6 can be operated at a suppressed current consumption and does not require a high-speed device incurring an increased apparatus

cost.

Further, by adopting a system sequence or flow of effecting an automatic picture position adjustment immediately before displaying a first picture in the picture display apparatus, it becomes possible to realize a system whereby an operator is unconscious of positional deviation of a display picture.

Hereinbelow, the operation of the embodiment will be described in further detail.

As mentioned above while referring to Figure 1, the picture display apparatus includes an A/D converter 1, a picture display unit drive circuit 2, a picture display unit 3, a display control circuit 4, a preset data memory 5 and a display position detection circuit 6. Inputted analog video signals Ra, Ga and Ba are converted into digital signals Rd, Gd and Bd by the A/D converter 1 based on a dot clock signal DCK, and the digital signals are inputted to the picture display unit drive circuit 2.

The picture display unit drive circuit 2 includes a picture memory 2m, and the converted digital video signals Rd, Gd and Bd are once stored in the picture memory 2m based on the dot clock signal DCK, and then read out based on a clock signal having a frequency different from that of the dot clock signal DCK to be processed so as to provide display

picture signals suitable for display on the picture display unit 3. According to the system organization, the timing of readout from the picture memory 2m is fixed, so that the picture display position on the picture display unit 3 is determined by the time when the digital video signals Rd, Gd and Bd are written in the picture memory based on the dot clock signal DCK. More specifically, if the writing in the memory 2m is effected at a horizontally early time, the display picture signal is outputted from the picture display unit drive circuit 2 at an early time to provide a picture display position shifted to a right side on the picture display unit 3. On the other hand, if the writing in the picture memory 2m is effected at a horizontally late time, the display picture outputted from the picture display unit drive circuit 2 at a later time to provide a picture display position shifted to a left side on the picture display unit 3. Similarly, the writing in the picture memory 2m at a vertically early time results in a picture display position shifted to a lower side and the writing in the memory 2m at a vertically late time results in a picture display position shifted to an upper side on the picture display unit 3.

The picture display unit drive circuit 2 also generates drive timing pulses (i.e., horizontal synchronizing pulses H, vertical synchronizing pulses

V and pixel clock signals CK) for the picture display unit 3. The video signals R, G and B prepared by processing in the picture display unit drive circuit 2 are inputted to the picture display unit 3 along with these timing pulses to display a picture on the picture display unit 3.

The timing of writing the digital video signals Rd, Gd and Bd in the picture memory is controlled by the display control circuit 4. The video signals R, G and B, the horizontal synchronizing signal H, the vertical synchronizing signal V and the pixel clock signal CK outputted from the picture display unit drive circuit 2, are also inputted to the display position detection circuit 6. The display position detection circuit 6 includes a counter for counting pixel clock pulses CK from a point of rise of the horizontal synchronizing signal H to detect a time HFC based on the number of clock pulses CK corresponding to a point of commencement of inputted video signals R, G, B and a time HRC based on the number of clock pulses CK corresponding to a point of termination (or absence) of the inputted video signals with respect to the horizontal position as shown in Figure 2. Further, the display position detection circuit 6 also includes a counter for counting the horizontal synchronizing pulses H from a point of rise of the vertical synchronizing signal V to detect a

time VFC based on the number of the horizontal synchronizing pulses H corresponding to a point of commencement of the video signals and a time VRC based on the number of horizontal synchronizing pulses H corresponding to a point of termination (or absence) of the inputted video signals. The position data HFC, HRC, VFC and VRC detected by the display position detection circuit 6 are inputted to the display control circuit 4, where differences of these values from set picture signal outputting timing values are determined. Based on the differences, the display control circuit 4 controls the timing of writing newly inputted digital signals Rd, Gd an Bd in the picture memory 2m contained in the picture display drive circuit 2. For example, at VIDEO, Figure 7 shows a case where a small difference on the order of several dots is present between the actual memory writing timing and the set memory writing timing, accordingly between the detected horizontal initial display position data HFC and a set horizontal initial display position data Phf. Based on the difference between HFC and Phf, the display control circuit 4 controls the timing of writing newly inputted digital data Rd, Gd and Bd in the picture memory 2m in the picture display unit drive circuit 2 according to an adjustment sequence illustrated in a flow chart of Figure 4 as will be described hereinafter.

On the other hand, in case where there is a large difference between the actual memory writing time and the set memory writing time, e.g., a difference of more than 304 dots exceeding a blanking period for inputted picture signals in an assumed case including totally 1328 dots within an interval between subsequent horizontal synchronizing signals and 1024 display dots, the video signal output from the picture display unit drive circuit 2 assumes a form as shown at VIDEO' in Figure 7. In Figure 7, Phr denotes a horizontal picture data output termination, whereas the writing time into the picture memory is deviated by more than on blanking period, the picture data outputted from the picture display unit drive circuit 2 beginning from time Phf and ending with time Phr is caused to include a blanking period therein. As a result, while the display position is actually remarkably deviated, the display position data HFC and HRC detected by the display position detection circuit 6 happen to be identical to set timing data of Phf and Phr, thus obstructing an accurate adjustment.

For obviating the above difficulty, a minimum degree within a necessary extent of preset data (e.g., ideal pixel memory writing timing data for each of representative resolution formats such as VGA, SVGA and XGA) are stored in the preset data memory 5, and one of such preset format data is stored in advance in

the picture display unit drive circuit 2 after judging the inputted signal format in the display control circuit 4, thereby by obviating the occurrence of an extreme positional deviation as shown at VIDEO' in Figure 7. After obviating such an extreme deviation, a minor degree of deviation as shown at VIDEO in Figure 7 is removed by controlling the timing for writing digital data in the pixel memory in the circuit 2 according to the adjustment flow of Figure 4.

Incidentally, in the above embodiment, picture signals in three types of R, G and B are inputted in the display position detection circuit 6, but it is possible to adopt a simple scheme of introducing only one type among R, G and B signals.

Figure 4 is a flowchart illustrating a display position adjustment sequence adopted in an embodiment of the picture display apparatus according to the present invention.

Referring to Figure 4, as a first step S1 of display position adjustment, horizontal and vertical display position data HFC, HRC, VFC and VRC are detected by the display position detection circuit 6. Then, at step S2, the set horizontal output commencement time Phf and vertical output commencement time Pvf from the picture display unit drive circuit 2 are compared with actual horizontal output

commencement time HFC and vertical output commencement time VFC, respectively, detected by the display position detection circuit 6. As a result of comparison, if the compared results are unequal, this means that the timing of writing digital data in the picture memory 2m is faster (i.e., too early; on the other hand, in case where the time is slower, no positional deviation in display commencement position is recognized as the data is present at the time after reading out of the memory and a prescribed processing of read data), and an operation at step S3 of adjusting a horizontal writing time Mh and a vertical writing time Mv respectively according to the following formulae:

$$Mh = Mhs + [HFC-Phf] \quad ...(1)$$

$$Mv = Mvs + [VFC-Pvf] \quad ...(2),$$

wherein Mhs and Mvs denote initial values of horizontal writing and vertical writing, respectively, in the picture memory 2m. If the comparison results at step S2 are equal, an operation at step S4 is performed.

At Step 4, the set horizontal output termination time Phr and vertical output termination time Pvr from the picture display unit drive circuit 2 are compared with actual horizontal output termination time HRC and vertical output termination time VRC, respectively, detected by the display

position detection circuit 6. As a result of comparison, if the compared results are unequal, this means that the timing of writing digital data in the picture memory 2m is slower (i.e., too late; on the other, in case where the time is faster, no positional deviation in display termination position is recognized as the data is present at the time after reading out of the memory and prescribed processing of read data), and an operator at step S5 of adjusting the horizontal writing time Mh and a vertical writing time Mr respectively according to the following formulae:

$$Mh = Mhs - [Phr-HRC] \quad ...(3)$$

$$Mv = Mvs - [Pvr-VRC] \quad ...(4).$$

If the comparison results at step S4 are equal, an operation at step S6 is performed.

At step S6, the display positions are so that:

$$Mh = Mhs \quad ....(5)$$

$$Mv = Mvs \quad ....(6).$$

Then, the display position adjustment is completed. On the other hand, it is also possible to place a step S7 where the initial values Mhs and Mvs are renewed according to the following formulae (7) and (8) based on the values of Mh and Mv according to the above formulae (3) and (4):

$$Mhs = Mh \quad ...(7)$$

$$Mvs = Mv \quad \ldots(8).$$

By effecting the above display position adjustment sequence just before a first picture display after turning on power supply to the picture display apparatus or just before display a first picture according to a new picture signal format after converting the previous picture signal format to the new picture signal format, it is possible to realize a display system wherein an operator is not conscious of a display picture positional deviation.

As described above, according to the present invention, by detecting a picture display position from picture data outputted from a picture display unit drive circuit, it becomes possible to effect an accurate display position detection on a picture display unit. Further, by using the result as a basis for controlling the timing for writing inputted video signals in a picture memory contained in the picture display unit drive circuit, it is possible to realize a good picture free from a partial lack of the picture.

Further, by disposing the display position detection unit in a later stage than the picture display unit drive circuit, i.e., in a drive environment of the picture display unit, the operation speed of the display position detection circuit can be lowered, thereby allowing an operation at a reduced

current consumption and adoption of a low-speed device for the circuit, leading to a reduced production cost.

WHAT IS CLAIMED IS:

1. A picture display apparatus for displaying a picture in response to inputted picture signals of arbitrary format, comprising:

a picture display apparatus having an arranged matrix of dots for picture display,

picture display unit drive means for converting inputted picture signals into display picture signals adapted for display on the picture display unit and generating drive timing signals for driving the picture display unit,

display position detection means for detecting a picture display position on the picture display unit based on the display picture signals and the drive timing signals, and

display position control means for controlling admission of the inputted picture signals to the picture display unit drive means based on the detected display position data from the display position detection means.

2. A picture display apparatus according to Claim 1, wherein said picture display unit drive means includes a picture memory for storing inputted picture signal admitted thereto, and generates a horizontal synchronizing signal, a vertical synchronizing signal and a pixel clock signal as the

drive timing signals.

3. A picture display apparatus according to Claim 2, wherein said display position detection means detects a horizontal commencement position of a picture displayed on the picture display unit in terms of a number of pixel clock signals from a rise of the horizontal synchronizing signal until first detection of the display picture signals, and detects a horizontal termination position of the picture in terms of a number of the pixel clock signals from the rise of the horizontal synchronizing signal until the termination of the display picture signals, respectively during one horizontal scanning period, and further detects a vertical commencement position of the picture in terms of a number of horizontal synchronizing signals from a rise of the vertical synchronizing signal until first detection of the display picture signals, and detects a vertical termination position of the picture in terms of a number of horizontal synchronizing signals from the rise of the vertical synchronizing signal until the termination of the display picture signals, respectively in one vertical scanning period, and

the display position control means controls a timing of admitting the inputted picture signals into the picture memory in the picture display unit drive

means, based on a difference between detected position data and set timing data for outputting display picture signals, thereby automatically adjusting a picture display position.

4. A picture display apparatus according to Claim 3, wherein said display position control means is further equipped with a preset data memory for storing ideal values for timing of writing in the picture memory respectively corresponding to a plurality of formats of the input picture signals, and also a means for judging a format of the inputted picture signals based on an inputted horizontal synchronizing signal and an inputted vertical synchronizing signal accompanying the inputted picture signals and for reading out the ideal value of the judged format of the inputted display picture signals.

ABSTRACT OF THE DISCLOSURE

Display position adjustment of a picture on a dot matrix-type picture display unit is automatically effected at a low current consumption and a low cost. This is accomplished by a picture display apparatus including such a picture display unit; picture display unit drive means for converting inputted picture signals into display picture signals adapted for display on the picture display unit and generating drive timing signals for driving the picture display unit; display position detection means for detecting a picture display position on the picture display unit based on the display picture signals and the drive timing signals; and display position control means for controlling admission of the inputted picture signals to the picture display unit drive means based on the detected display position data from the display position detection means.

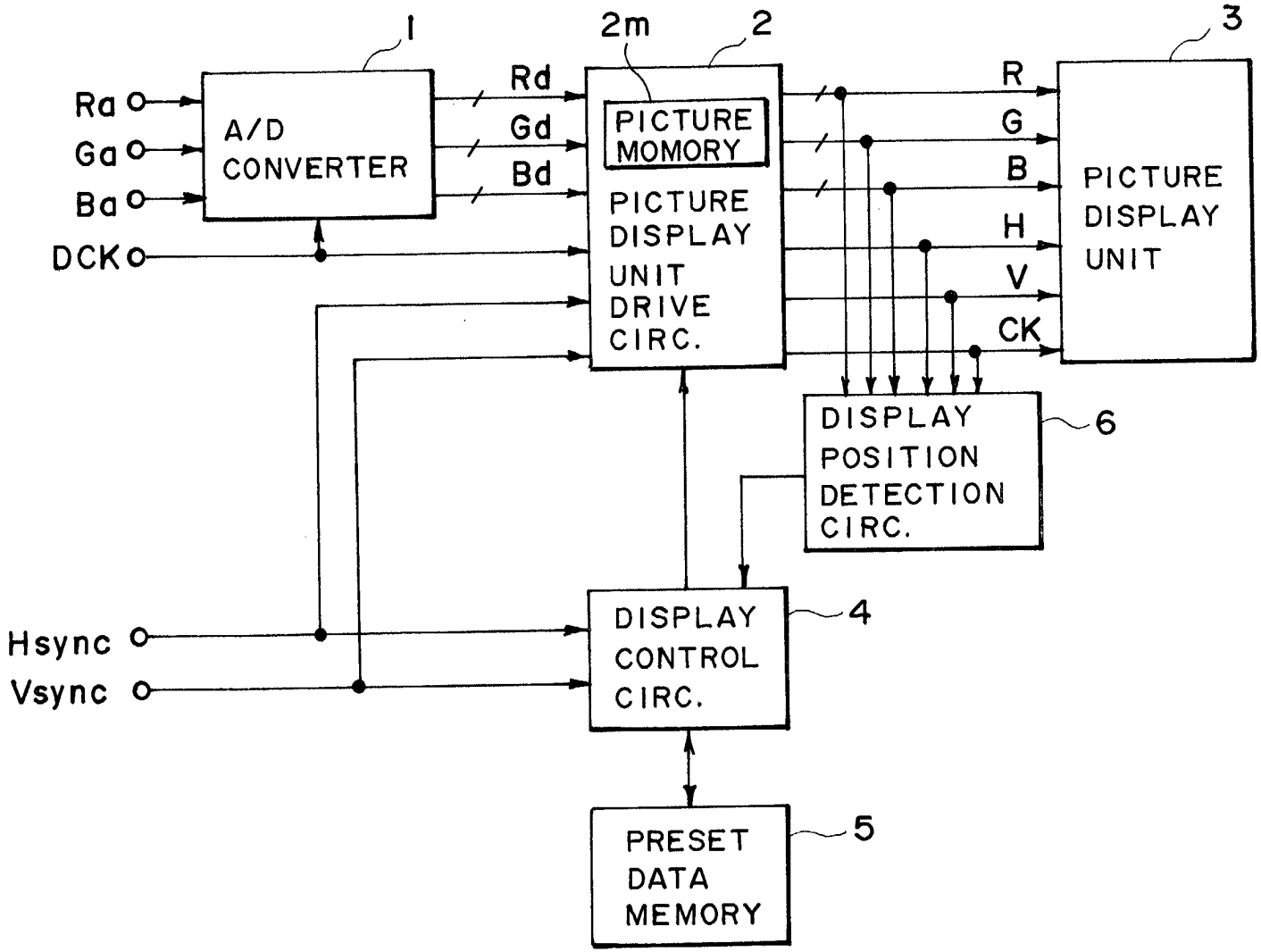

FIG. 1

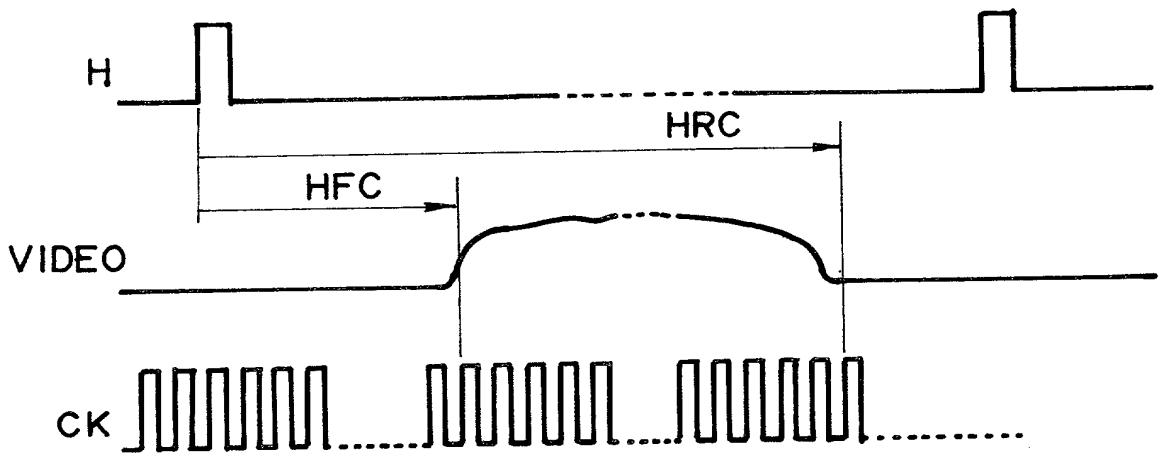

FIG. 2

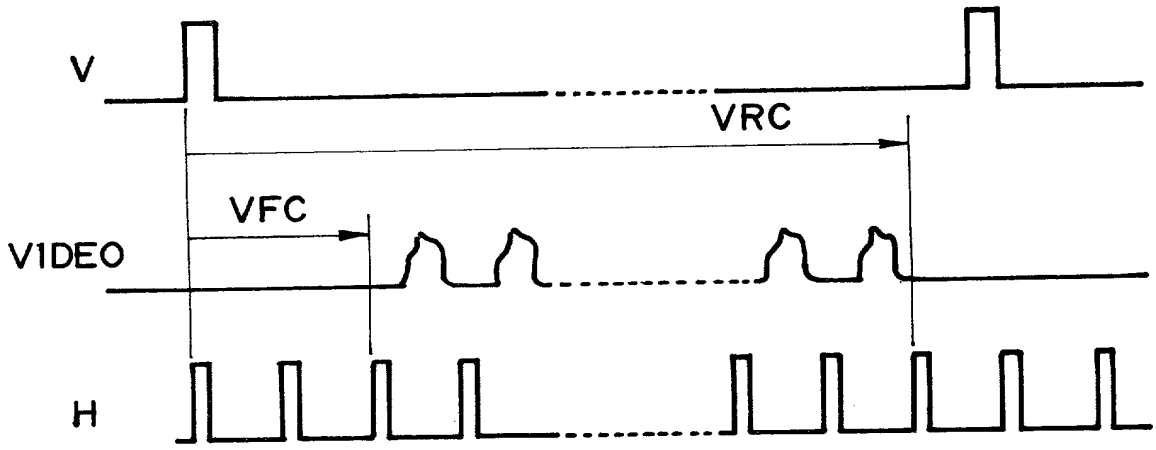

FIG. 3

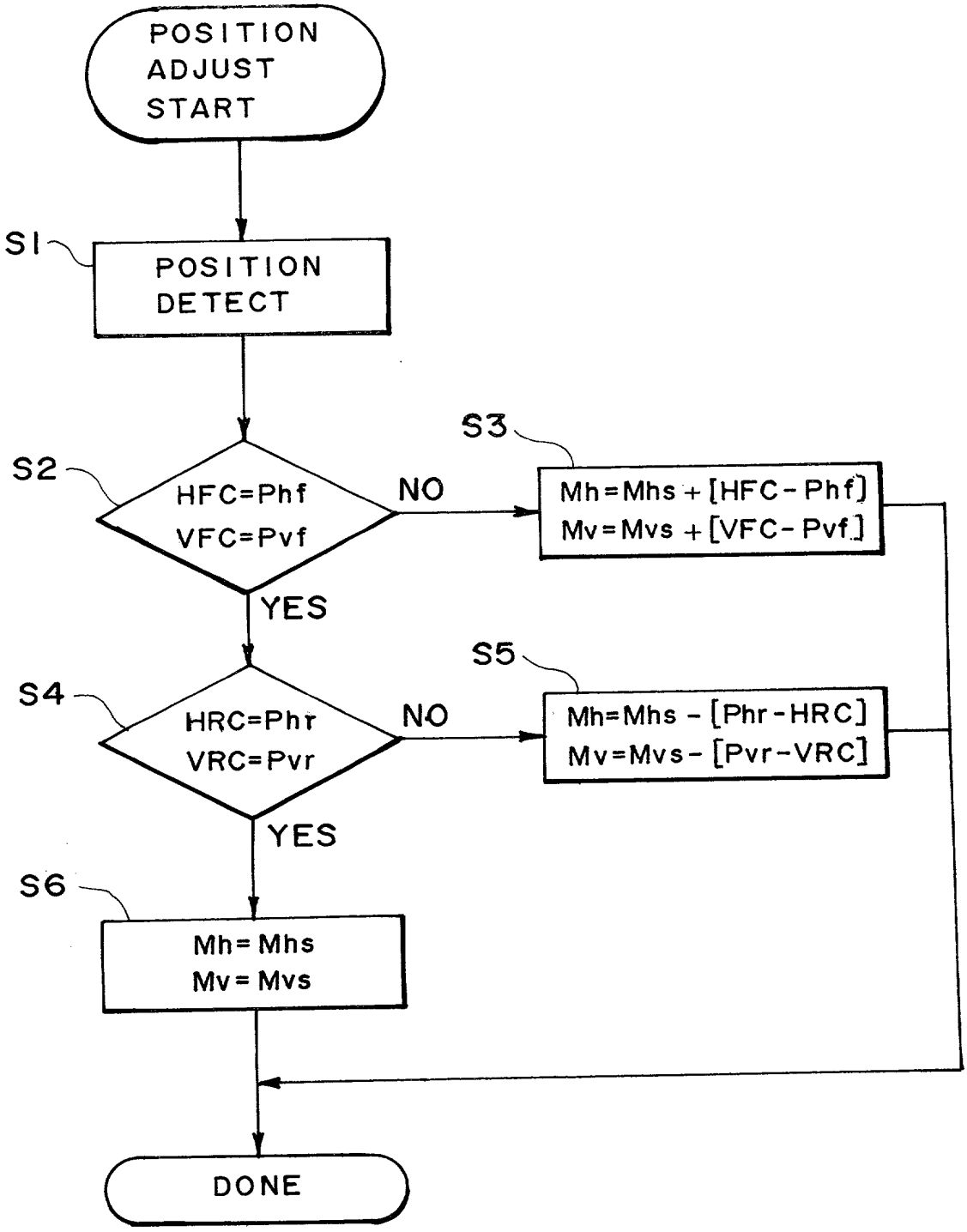
POSITION ADJUST START
S1
POSITION DETECT
S2
HFC=Phf
VFC=Pvf
NO
S3
Mh=Mhs+[HFC-Phf]
Mv=Mvs+[VFC-Pvf]
YES
S4
HRC=Phr
VRC=Pvr
NO
S5
Mh=Mhs-[Phr-HRC]
Mv=Mvs-[Pvr-VRC]
YES
S6
Mh=Mhs
Mv=Mvs
DONE

FIG. 4

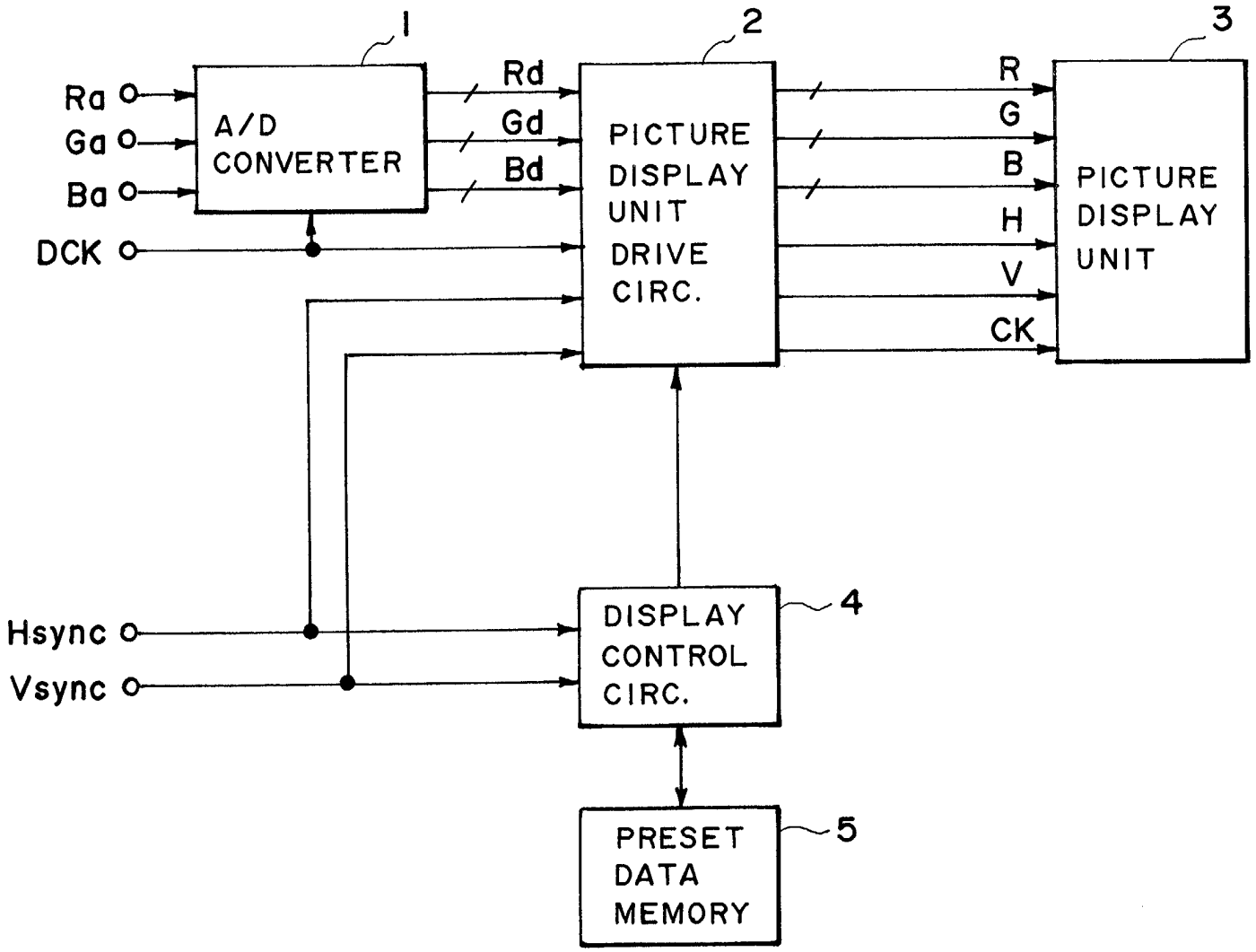
1
2
3
Ra
Ga
Ba
DCK
A/D CONVERTER
Rd
Gd
Bd
PICTURE DISPLAY UNIT DRIVE CIRC.
R
G
B
H
V
CK
PICTURE DISPLAY UNIT
Hsync
Vsync
DISPLAY CONTROL CIRC.
4
PRESET DATA MEMORY
5

FIG. 5

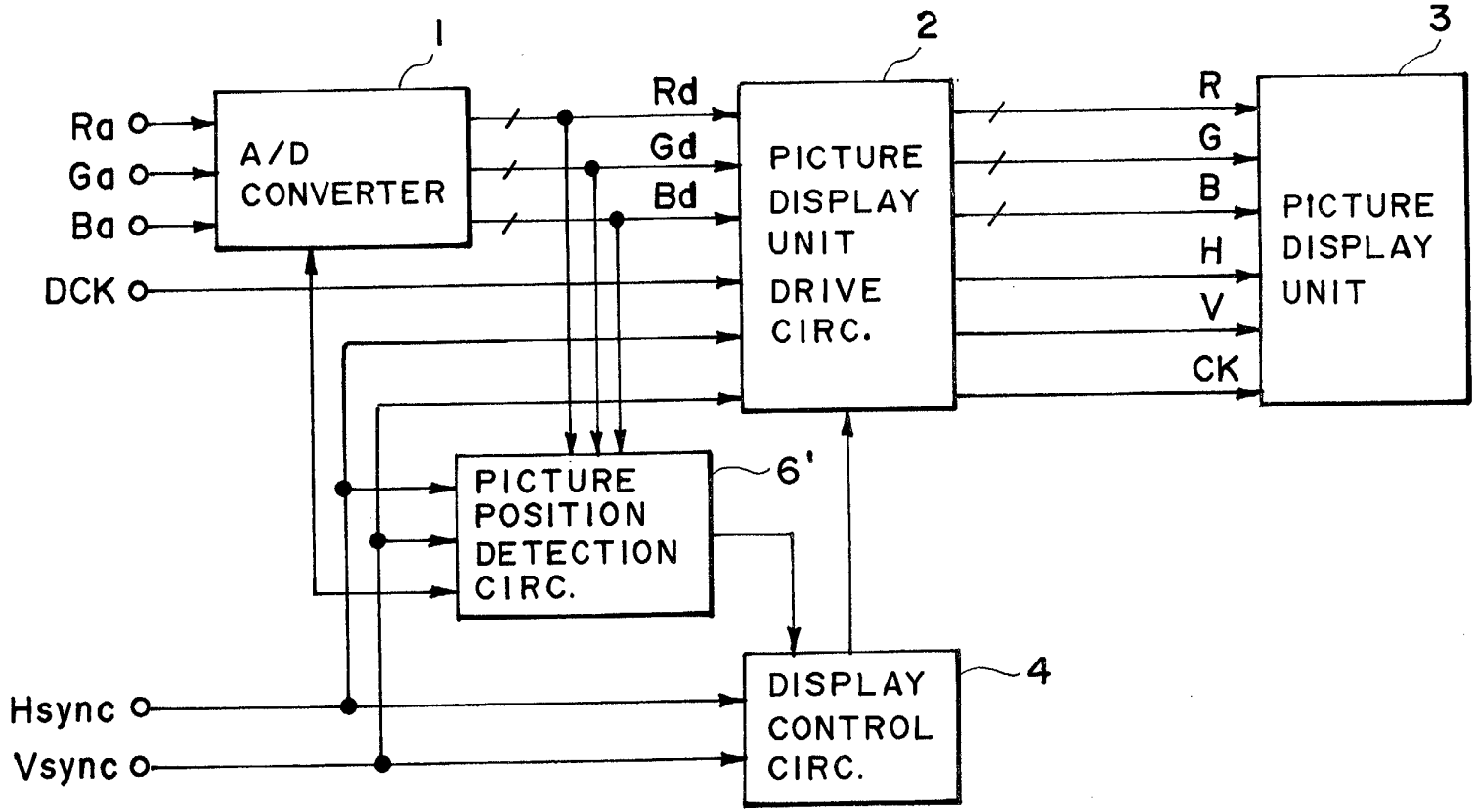

FIG. 6

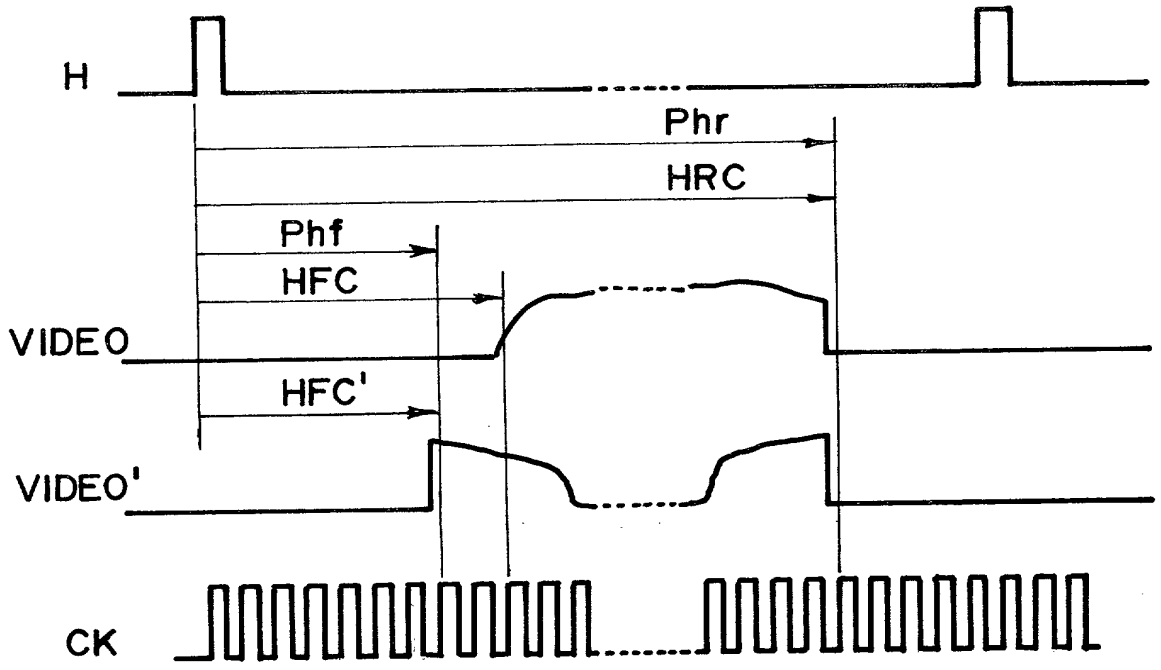

FIG. 7

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled PICTURE DISPLAY APPARATUS,

the specification of which [X] is attached hereto [ ] was filed on _____ as United States Application No. or PCT International Application No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or §365(b), of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designates at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed:

Country	Application No.	Filed (Day/Mo./Yr.)	(Yes/No) Priority Claimed
JAPAN	11-022752	29/JANUARY/1999	Yes

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Application No.	Filed (Day/Mo./Yr.)	Status (Patented, Pending, Abandoned)

I hereby appoint the practitioners associated with the firm and Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to the address associated with that Customer Number:

FITZPATRICK, CELLA, HARPER & SCINTO
Customer Number: 05514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole or First Inventor AKIHIRO OUCHI

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